Please amend the claims as follows:

Please cancel claims 1-40 and 59-71

Please add claims 72 to 197:

72. (new) A memory element, comprising:

a programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material, said electrical contact having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said second region being adjacent to said programmable resistance material, said first region being remote to said programmable resistance material, said electrical contact comprising a conductive layer, said second region being a modified portion of said conductive layer.

73. (new) The memory element of claim 72, wherein said second region is doped differently from said first region.

74. (new) The memory element of claim 72, wherein said second region has a different dopant type from said first region.

75. (new) The memory element of claim 72, wherein said second region has a different dopant concentration from said first region.

76. (new) The memory element of claim 72, wherein substantially all of said electrical communication occurs through at least a portion of an edge of said electrical contact.

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77. (new) The memory element of claim 72, wherein said electrical contact has at least a portion of an edge adjacent to said programmable resistance material, wherein substantially all of the remainder of said electrical contact being remote to said programmable resistance material.

78. (new) The memory element of claim 76, wherein said at least a portion of said edge has a dimension in at least one direction between 50 and 1000 Angstroms.

79. (new) The memory element of claim 72, wherein at least a portion of said electrical contact is formed over a dielectric layer.

80. (new) The memory element of claim 72, wherein at least a portion of said electrical contact is formed over a sidewall surface of a dielectric layer.

81. (new) The memory element of claim 72, wherein said electrical contact comprises a conductive sidewall layer formed over a sidewall surface of a dielectric layer.

82. (new) The memory element of claim 72, wherein said electrical contact comprises a conductive sidewall spacer formed over a sidewall surface of a dielectric layer.

83. (new) The memory element of claim 72, wherein said electrical contact comprises a conductive liner formed over the sidewall surface and bottom surface of an opening formed in a dielectric layer.

84. (new) The memory element of claim 72, wherein said electrical contact includes one or more raised portions extending to terminal ends adjacent to said programmable resistance material.

85. (new) The memory element of claim 72, wherein said electrical contact comprises polysilicon.

86. (new) The memory element of claim 72, said electrical contact and said programmable resistance material have an area of contact having a dimension in at least one direction which is between 50 Angstroms and 1000 Angstroms.

87. (new) The memory element of claim 72, wherein said programmable resistance material comprises a phase change material.

88. (new) A memory element, comprising:

a programmable resistance material; and

an electrical contact in electrical communication with programmable resistance material, said electrical contact having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said second region being adjacent to said programmable resistance material, said first region being remote to said programmable resistance material, said electrical contact comprising polysilicon.

89. (new) The memory element of claim 88, wherein said second region is doped differently from said first region.

90. (new) The memory element of claim 88, wherein said second region has a different dopant type from said first region.

91. (new) The memory element of claim 88, wherein said second region has a different dopant concentration from said first region.

92. (new) The memory element of claim 88, wherein substantially all of said electrical communication occurs through at least a portion of an edge of said electrical contact.

93. (new) The memory element of claim 88, wherein said at least a portion of said edge has a dimension in at least one direction which is between 50 Angstroms and 1000 Angstroms.

94. (new) The memory element of claim 88, wherein said electrical contact and said programmable resistance material has an area of contact having a dimension between 50 Angstroms and 1000 Angstroms in at least one direction.

95. (new) The memory element of claim 88, wherein said electrical contact includes one or more raised portions extending to terminal ends adjacent to said programmable resistance material, substantially all of said electrical communication occurring through at least a portion of the surface of at least one of said raised portions.

96. (new) The memory element of claim 88, wherein said electrical contact has at least a portion of an edge adjacent to said programmable resistance material, substantially all of the remainder of said electrical contact being remote to said programmable resistance material.

97. (new) The memory element of claim 88, wherein at least a portion of said electrical contact is formed over at least a portion of a dielectric layer.

98. (new) The memory element of claim 88, wherein at least a portion of said electrical contact is formed over a sidewall surface of a dielectric layer.

99. (new) The memory element of claim 88, wherein said electrical contact comprises a conductive sidewall layer formed over a sidewall surface of a dielectric layer.

100. (new) The memory element of claim 88, wherein said electrical contact comprises a conductive sidewall spacer formed over a sidewall surface of a dielectric layer.

101. (new) The memory element of claim 88, wherein said electrical contact comprises a conductive liner formed over a sidewall surface and a bottom surface of an opening of a dielectric layer.

102. (new) The memory element of claim 88, wherein said first region comprises a first conductive layer and said second region comprises a second conductive layer.

103. (new) The memory element of claim 88, wherein said programmable resistance material comprises a phase change material.

104. (new) A memory element, comprising:

a programmable resistance programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material, said electrical contact having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said second region being adjacent to said programmable resistance material, said first region being remote to said programmable resistance material, said first region being doped differently from said second region.

105. (new) The memory element of claim 104, wherein said first region has a different dopant concentration from said second region.

106. (new) The memory element of claim 104, wherein said first region has a different dopant type from said second region.

107. (new) The memory element of claim 104, wherein substantially all of said electrical communication occurs through at least a portion of an edge of said electrical contact.

108. (new) The memory element of claim 104, wherein said at least a portion of said edge includes one or more raised portions extending to terminal ends adjacent to said programmable resistance material.

109. (new) The memory element of claim 104, wherein substantially of said electrical communication occurs through at least one of said terminal ends.

110. (new) The memory element of claim 104, wherein said electrical contact has an edge portion adjacent to said programmable resistance material, substantially all of the remainder of said electrical contact being remote to said programmable resistance material.

111. (new) The memory element of claim 104, wherein said electrical contact and said programmable resistance material have an area of contact having at least one dimension in at least one direction which is between 50 Angstroms and 1000 Angstroms.

112. (new) The memory element of claim 104, wherein at least a portion of said electrical contact formed is formed over at least a portion of a dielectric layer.

113. (new) The memory element of claim 104, wherein at least a portion of said electrical contact is formed over a sidewall surface of a dielectric layer.

114. (new) The memory element of claim 104, wherein said electrical contact comprises a sidewall layer formed over a sidewall surface of a dielectric layer.

115. (new) The memory element of claim 104, wherein said electrical contact comprises a conductive sidewall spacer formed over a sidewall surface of a dielectric layer.

116. (new) The memory element of claim 104, wherein said electrical contact comprises a conductive liner formed over the sidewall surface and bottom surface of an opening in a dielectric layer.

117. (new) The memory element of claim 104, wherein said first region comprises a first conductive layer and said second region comprises a second conductive layer.

118. (new) The memory element of claim 104, wherein said programmable resistance material comprises a phase change material.

119. (new) A memory element, comprising:

a substrate;

a programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material and said substrate, substantially all of said electrical communication between said electrical contact and said programmable resistance material occurring through at least a portion of an edge of said electrical contact, said electrical contact having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said second region adjacent to said programmable resistance material and spacedly disposed from said substrate, said first region being spacedly disposed from said programmable resistance material.

120. (new) The memory element of claim 119, wherein said second region being separated from said substrate by said first region.

121. (new) The memory element of claim 119, wherein said programmable resistance material and said electrical contact have an area of contact between said electrical contact and said programmable resistance material, said electrical contact having a ratio D2:DT > 5:6 where DT is the distance from said substrate to the lowest point of said area of contact and D2 is the distance from the substrate to the lowest point of said second region.

122. (new) The memory element of claim 119, wherein substantially all of said second region is above substantially all of said first region.

123. (new) The memory element of claim 119, wherein substantially all of said first and second regions forming a serially coupled electrical pathway between said substrate and said programmable resistance material.

124. (new) The memory element of claim 119, wherein said electrical contact and said programmable resistance material have an area of contact, said area of contact having a dimension between 50 Angstroms and 1000 Angstroms in at least one direction.

125. (new) The memory element of claim 119, wherein said first region is adjacent to said substrate.

126. (new) The memory element of claim 119, wherein said at least a portion of said edge includes one or more raised portions extending to terminal ends adjacent to said programmable resistance material.

127. (new) The memory element of claim 119, wherein said first region is a top portion of said electrical contact and said second region is a bottom portion of said second contact.

128. (new) The memory element of claim 119, wherein at least a portion of said electrical contact is formed over at least a portion of a dielectric layer.

129. (new) The memory element of claim 119, wherein said electrical contact is formed over a sidewall surface of a dielectric layer.

130. (new) The memory element of claim 119, wherein said electrical contact comprises a sidewall layer formed over dielectric sidewall surface.

131. (new) The memory element of claim 119, wherein said electrical contact comprises a conductive sidewall spacer formed over a sidewall surface of a dielectric layer.

132. (new) The memory element of claim 119, wherein said electrical contact comprises a conductive sidewall liner formed over a sidewall surface and a bottom surface of an opening in a dielectric layer.

133. (new) The memory element of claim 119, wherein said electrical contact comprises a conductive layer, said second region being a modified portion of said conductive layer.

134. (new) The memory element of claim 119, wherein said first region comprises a first conductive layer and said second region comprises a second conductive layer.

135. (new) The memory element of claim 119, wherein said programmable resistance material comprises a phase change material.

136. (new) The memory element of claim 119, wherein said first region comprises at least one member selected from the group consisting of n-type polysilicon, p-type polysilicon, n-type silicon carbide, p-type silicon carbide, titanium-tungsten, tungsten silicide, tungsten, molydenum, and titanium nitride.

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137. (new) The memory element of claim 119, wherein said second region comprises at least one member selected from the group consisting of n-type polysilicon, p-type polysilicon, n-type silicon carbon compounds and/or alloys, p-type silicon carbon compounds and/or alloys, titanium carbon-nitride, titanium aluminum nitride, titanium silicon-nitride, carbon, and titanium nitride.

138. (new) A memory element comprising, comprising:

a programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material, substantially all of said electrical communication occurring through at least a

portion of an edge of said electrical contact, said electrical contact having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said second region being adjacent to said programmable resistance material while said first region is remote to said programmable resistance material, at least a portion of said electrical contact being formed over at least a portion of a dielectric layer.

B1 Cont

139. (new) The memory element of claim 138, wherein said dielectric layer has a sidewall surface, said electrical contact being formed over said sidewall surface.

140. (new) The memory element of claim 139, wherein said electrical contact comprises a conductive sidewall layer formed over said sidewall surface of said dielectric layer.

141. (new) The memory element of claim 139, wherein said electrical contact comprises a conductive sidewall spacer formed over said sidewall surface of said dielectric layer.

142. (new) The memory element of claim 139, wherein said electrical contact comprises a conductive sidewall liner, a

portion of said conductive liner formed over said sidewall surface of said dielectric layer.

143. (new) The memory element of claim 138, wherein said at least a portion of said edge includes one or more raised portions extending to one or more terminal ends adjacent to said programmable resistance material.

144. (new) The memory element of claim 143, wherein substantially all of said electrical communication occurs through at least one of said terminal ends.

145. (new) The memory element of claim 138, wherein said electrical contact comprises a conductive material, said second region being a modified portion of said conductive material.

146. (new) The memory element of claim 138, wherein said first region comprises a first conductive layer and said second region comprises a second conductive layer.

147. (new) The memory element of claim 138, wherein said programmable resistance material comprises a phase change material.

148. (new) The memory element of claim 138, wherein said first region comprises at least one member selected from the group consisting of n-type polysilicon, p-type polysilicon, n-type silicon carbide, p-type silicon carbide, titanium-tungsten, tungsten silicide, tungsten, molydenum, and titanium nitride.

149. (new) The memory element of claim 138, wherein said second region comprises at least one member selected from the group consisting of n-type polysilicon, p-type polysilicon, n-type silicon carbon compounds and/or alloys, p-type silicon carbon compounds and/or alloys, titanium carbon-nitride, titanium aluminum nitride, titanium silicon-nitride, carbon, and titanium nitride.

150. (new) A memory element, comprising:

a programmable resistance material; and

a conductive sidewall spacer formed over a sidewall surface of a dielectric layer, said conductive spacer in electrical communication with said programmable resistance material, substantially all of said electrical communication between said conductive sidewall spacer and said programmable resistance material occurring through at

least a portion of an edge of said conductive spacer, said electrical contact having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said second region being adjacent to said programmable resistance material, said first region being remote to said programmable resistance material.

151. (new) The memory element of claim 150, wherein said at least a portion of said edge includes one or more raised portions extending to terminal ends adjacent to said programmable resistance material.

152. (new) The memory element of claim 151, wherein substantially all of said electrical communication occurs through at least one of said terminal ends.

153. (new) The memory element of claim 150, wherein said at least a portion of said edge has a dimension between 50 and 1000 Angstroms in at least one direction.

154. (new) The memory element of claim 150, wherein said programmable resistance material comprises a phase change material.

155. (new) The memory element of claim 150, wherein said programmable resistance material comprises a chalcogen element.

156. (new) The memory element of claim 150, wherein said conductive spacer comprises a conductive layer, said second region being a modified portion of said conductive layer.

157. (new) The memory element of claim 150, wherein said first region comprises a first conductive layer and said second region comprises a second conductive layer.

Cont.

158. (new) A memory element, comprising:

a programmable resistance material; and

a conductive liner that lines the sidewall and bottom surfaces of an opening of a dielectric material, said conductive liner in electrical communication with said programmable resistance material, substantially all of said electrical communication between said conductive liner and said programmable resistance material occurring through at least a portion of an edge of said conductive liner, said conductive liner having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said

second region being adjacent to said programmable resistance material, said first region being remote to said programmable resistance material.

159. (new) The memory element of claim 158, wherein said at least a portion of said edge has a dimension between 50 Angstroms and 1000 Angstroms in at least one direction.

160. (new) The memory element of claim 158, wherein said conductive liner and said programmable resistance material have an area of contact that is annular.

161. (new) The memory element of claim 158, wherein said conductive liner and said programmable resistance material have an area of contact that is linear.

162. (new) The memory element of claim 158, wherein said conductive liner is cup-shaped.

163. (new) The memory element of claim 158, wherein said conductive liner is u-shaped.

164. (new) The memory element of claim 158, wherein said at least said portion of said edge includes one or more raised

portions extending to terminal ends adjacent to said programmable resistance material.

165. (new) The memory element of claim 158, wherein said conductive liner comprises a conductive layer, said second region being a modification of said conductive layer.

166. (new) The memory element of claim 158, wherein said first region comprises a first conductive layer and said second region comprises a second conductive layer.

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167. (new) The memory element of claim 158, wherein said first region is doped differently from said second region.

168. (new) The memory element of claim 158, wherein said programmable resistance material comprises a phase change material.

169. (new) The memory element of claim 158, wherein said programmable resistance material comprises a chalcogen element.

170. (new) A memory element, comprising:

a programmable resistance material; and

a cup-shaped electrical contact in electrical communication with said programmable resistance material, wherein substantially all of said electrical communication occurring through at least a portion of a rim of said electrical contact, said electrical contact including a first portion having a first resistivity and a second portion having a second resistivity greater than said first resistivity, said second portion being adjacent said programmable resistance material, said first portion being remote to said programmable resistance material.

171. (new) The memory element of claim 170, wherein said at least a portion of said rim is adjacent said programmable resistance material.

172. (new) The memory element of claim 170, wherein said at least a portion of said rim includes one or more raised portions extending to one or more terminal ends adjacent said programmable resistance material.

173. (new) The memory element of claim 172, wherein substantially all of said electrical communication between

said electrical contact and said programmable resistance material occurs through at least one of said terminal ends.

174. (new) The memory element of claim 170, wherein said cup-shaped contact comprises a conductive layer, said second region being a modification of said conductive layer.

175. (new) The memory element of claim 170, wherein said first region comprises a first conductive layer and said second region comprises a second conductive layer.

176. (new) The memory element of claim 170, wherein said programmable resistance material comprises a phase change material.

177. (new) A memory element, comprising:

a programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material, said electrical contact having at least a portion of an edge that includes one or more raised portions, substantially all of said electrical communication between said electrical contact and said programmable resistance material occurring through

at least a portion of the surface of at least one of said raised portions, said electrical contact having at least a first region with a first resistivity and a second region with a second resistivity greater than said first resistivity, said second region adjacent said programmable resistance material, said first region remote to said programmable resistance material.

B1 cont.

178. (new) The memory element of claim 177, wherein said raised portions extend to terminal ends adjacent to said programmable resistance material, substantially all of said electrical communication occurring through at least one of said terminal ends.

179. (new) The memory element of claim 177, wherein at least a portion of said electrical contact is formed over a sidewall surface of a dielectric layer.

180. (new) The memory element of claim 177, wherein said electrical contact comprises a sidewall layer formed over a sidewall surface of a dielectric layer.

181. (new) The memory element of claim 177, wherein said electrical contact comprises a conductive sidewall spacer formed over a sidewall surface of a dielectric layer.

182. (new) The memory element of claim 177, wherein said electrical contact comprises a conductive sidewall liner formed over a sidewall surface and a bottom surface of an opening in a dielectric layer.

183. (new) The memory element of claim 177, wherein said electrical contact is cup-shaped.

184. (new) The memory element of claim 178, wherein at least one of said terminal ends has a dimension between 50 Angstroms and 1000 Angstroms in at least one direction.

185. (new) The memory element of claim 177, wherein said electrical contact comprises a conductive layer, said second region being a modified portion of said conductive layer.

186. (new) The memory element of claim 177, wherein said first region comprises a first conductive layer and said second region comprises a second conducive layer.

187. (new) The memory element of claim 177, wherein said raised portions taper as they extend from said at least a portion of said edge.

188. (new) The memory element of claim 177, wherein said raised portions have substantially straight sidewalls.

189. (new) The memory element of claim 177, wherein said programmable resistance material comprises a phase change material.

190. (new) A memory element, comprising:

a programmable resistance programmable resistance material; and

an electrical contact in electrical communication with said programmable resistance material, substantially all electrical contact being through at least a portion of an edge of said electrical contact, said at least a portion of said edge at least partially encircling said programmable resistance material, said electrical contact having a first portion with a first resistivity and a second portion with a second resistivity greater than said first resistivity, said second portion being adjacent said programmable

resistance material, said first portion being remote said programmable resistance material.

191. (new) The memory element of claim 190, wherein said at least a portion of said edge completely encircles said programmable resistance material.

192. (new) The memory element of claim 190, wherein said electrical contact comprises a conductive layer, said second region being a modified portion of said conductive layer.

B1 cont.

193. (new) The memory element of claim 190, wherein said first portion comprises a first conductive layer and said second portion comprises a second conductive layer.

194. (new) The memory element of claim 190, wherein said second region is doped differently from said first region.

195. (new) The memory element of claim 190, wherein said programmable resistance material comprises a phase change material.

196 (new) The memory element of claim 190 wherein said programmable resistance material comprises a chalcogen element.

197. (new) The memory element of claim 190, wherein said first region comprises at least one member selected from the group consisting of n-type polysilicon, p-type polysilicon, n-type silicon carbide, p-type silicon carbide, titanium-tungsten, tungsten silicide, tungsten, molydenum, and titanium nitride.

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~~196~~. (new) The memory element of claim 188, wherein said second region comprises at least one member selected from the group consisting of n-type polysilicon, p-type polysilicon, n-type silicon carbon compounds and/or alloys, p-type silicon carbon compounds and/or alloys, titanium carbon-nitride, titanium aluminum nitride, titanium silicon-nitride, carbon, and titanium nitride.